This 8051 IP is an economical, high-performance core that implements an 8051-like 8-bit microcontroller that executes all ASM51 instructions. The core provides hardware and software interrupt, an interface for serial communication, two timers, an Intel-compatible interrupt scheme, parallel I/O ports. ASIC implementation data shows it to offer competitive performance and area results, requiring for example about 10K gates for 100 MHz for 0.18u process.

This design is strictly synchronous, with positive-edge clocking and a synchronous reset. DFT features e.g. scan insertion is straightforward. System development is facilitated through support by Keil's C51 integrated development environment.

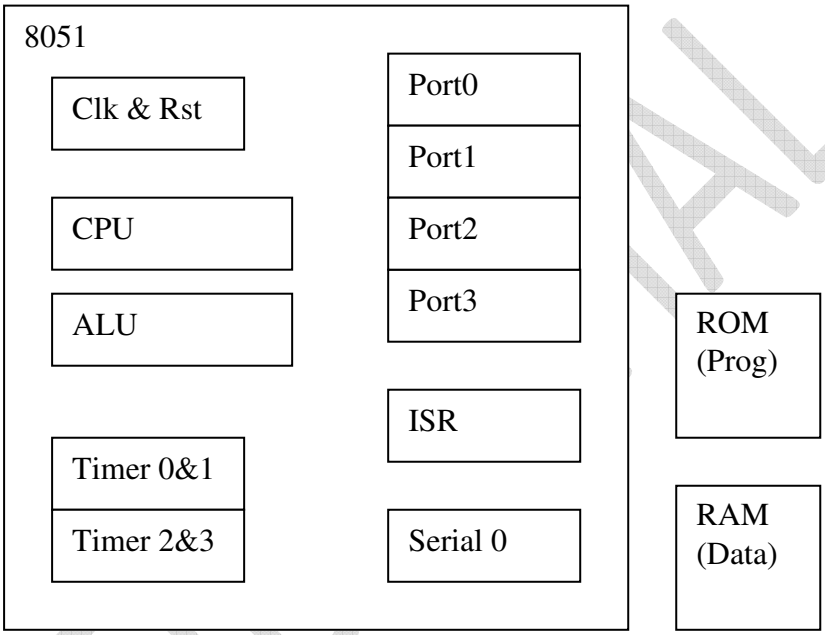
Features

- Fully synchronous circuit design up to 100MHz
- OP code compatible to original Intel 8051 device
- ALU performs 8-bit arithmetic, multiplication and division, and Boolean manipulations
- Two 16-bit Timer/Counters
- 32-bit Input/Output ports
    - Four 8-bit I/O ports
    - Alternate port functions such as external interrupts and serial interface are separated, providing extra port pins when compared with the standard 8051
- Executed instructions in 1-4 clock cycles depending on the number of operands
- Separate RAM and ROM data/address busses
- Parametrizeable number of timer and UART units
- Interrupt Controller with two priority levels and five sources
- Internal Data Memory Interface can address up to 256 bytes of Read/Write Data Memory Space
- Can address up to 64Kb of Program Memory and up to 64Kb of Data Memory
- Debugging support and debugging software with interface to Keil C51 tools

Applications

Symmid MC8051 is suitable as the preferred controller in applications and products requiring low power consumption, high-speed control systems, and mixed-signal SoC applications due to its ease of implementation and many customizable features.

Block Diagram



Functional Description

The core is partitioned into modules as shown in the block diagram and described below.

CPU and ALU

Fetches instructions from program memory and uses RAM or SFRs as operands. Provides the ALU for 8-bit arithmetic, logic, multiplication and division operations and Boolean manipulations. The RAM and SFR interface can address up to 256 bytes of Read/Write Data Memory Space and built-in and off-core Special Function Registers. The memory interface can address from 64K bytes of Program Memory and of Data Memory

Ports

Ports p0 – p3 are Special Function Registers that can be observed on the corresponding pins. The CPU can output or read data through any of these ports unless a port is used for an alternate purpose.

Timers 0 and 1 (2 and 3)

Each of these two 16-bit registers can be configured as a timer or a counter. A timer is incremented every machine cycle, meaning it counts up after every 12 oscillator periods. A counter is incremented when a falling edge is recognized at a pin. Four operating modes are available for timers 0 and 1, selectable through two SFRs. The core is customizable up to 4 timers.

Serial 0

The serial buffer consists of two separate registers, a transmit buffer and receive buffer, and it can simultaneously transmit and receive data. It can also buffer one byte of received data, preventing the received data from being lost if the CPU reads the first byte before transmission of the second byte is finished.

Interrupt Service Routine Unit

The core provides five interrupt sources. Two external interrupts are edge- or level-sensitive. Two internal interrupts are associated with Timer 0 and Timer 1; the third with the Serial Port.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) format:

- Verilog HDL RTL source code (ASICs) or encrypted post-synthesis EDIF netlist (FPGAs)
- Simulation script, vectors, and expected results
- Synthesis script (ASICs) or place and route script (FPGAs)
- Comprehensive user documentation, including detailed specifications and a system integration guide

