The SD925 is a constant frequency, current mode, step-down DC-DC controller. It provides system flexibility by allowing settings of the current limit with external resistor. The output voltage can be configured using 2 external resistors. SD925 includes safety features e.g. short-circuit protection, output overvoltage protection and input overvoltage protection. Operating frequencies at 550kHz allows the use of a smaller inductor. The SD925 is packaged in TSOT6 package.

Features

- Wide input voltage range: 5.5 V to 15 V
- Wide output voltage range: 2V to 12V
- Up to 92% efficiency
- Output current range: 2A max
- Slow and Fast Clock (550kHz)
- Drive External P-Gate
- External Sense Resistor
- COMP pin (o/p of error amplifier)
- FB pin (feedback from output voltage)
- Short-circuit and overvoltage protection

Applications

- Wireless devices
- to 3-cell Li-Ion battery-powered applications
- Set-top boxes
- Processor core power supplies
- Hard disk drives

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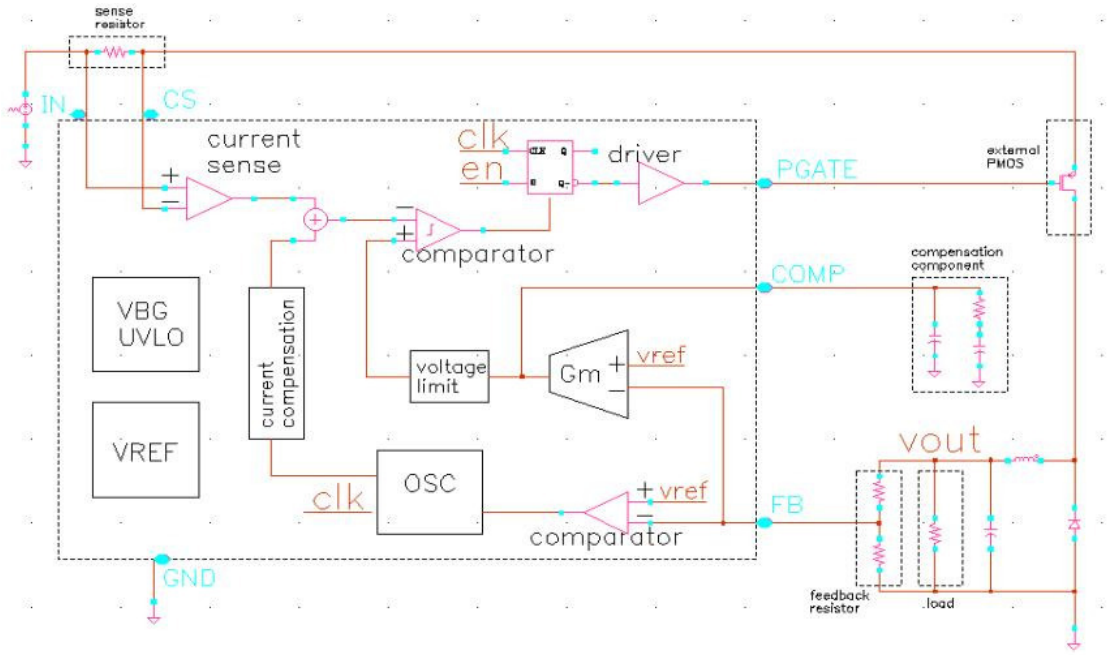
Block Diagram



Pin Assignments

Pin Name	Pad	Description
CS	Analog	Current sense resistor is connected between CS and IN. Current limit is set with proper resistor value.
GND	Ground	Analog ground
VIN		Power input range from 5.5V to 15V
PGATE	Analog	Driver output to drive external pmos
COMP	Analog	Output of a Gm transconductance error amp
FB	Analog	Output voltage with voltage divider resistor is feedback. FB voltage is regulated at 0.8V

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Functional Description

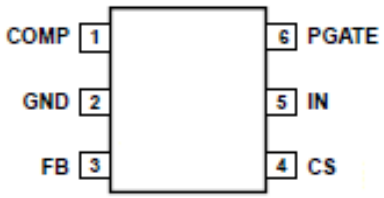
Symmid SD925 is a constant frequency (550 kHz), current-mode buck controller. PGATE drives the gate of the external P-channel FET. The duty cycle of the external FET dictates the output voltage and the current supplied to the load.

The peak inductor current is measured across the external sense resistor, while the system output voltage is fed back through an external resistor divider to the FB pin.

At the start of every oscillator cycle, PGATE turns on the external FET, causing the inductor current, and therefore the current sense amplifier voltage, to increase. The inductor current increases until the current amplifier voltage equals the voltage at the COMP pin. This resets the internal flip-flop, causing PGATE to go high and turning off the external FET. The inductor current decreases until the beginning of the next oscillator period.

The voltage at the COMP node is the output of the internal error amplifier. The negative input of the error amplifier is the output voltage scaled by an external resistive divider, and the positive input to the error amplifier is driven by a 0.8 V band gap reference. An increase in the load current causes a small drop in the feedback voltage, in turn causing an decrease in the COMP voltage and, therefore, the duty cycle. The resulting increase in the on time of the FET

Packaging



6-pin TSOT

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